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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,953	12/31/2001	Chris Haywood	6979-0026	8426

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 09/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,953	HAYWOOD, CHRIS	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Page 5 lines 23-24, "The FIFO circuit 402 includes a tail FIFO memory 408, a head FIFO memory 410 and a multiplexer (mux) 412", should be -- The FIFO circuit 402 includes a tail FIFO memory 410, a head FIFO memory 408 and a multiplexer (mux) 412-- according to figure 4.

Page 11 line 11, "the method proceeds to block 812" should be -- the method proceeds to block 810 -- according to figure 8.

Page 11 line 13, "the method proceeds to block 818" should be -- the method proceeds to block 816 -- according to figure 8.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-11 rejected under 35 U.S.C. 102(e) as being anticipated by Bass et al (US PAT. 6,557,053 hereinafter Bass).

Regarding claim 1, Bass discloses a caching system, i.e. a bandwidth conserving queue manager (10, figure 1) comprising a tail FIFO memory, i.e., input FIFO queue (14, figure 1) having a tail input to receive incoming data (12, figure 1) from a outside source (col. 1 line 66 through col. 2 line 3), and a tail output to output the incoming data, i.e., data (16, figure 1) is outputted from the input FIFO buffer 14 to a memory interface (18) and to a multiplexor (20) (col. 2 lines 3-5), a memory, i.e., memory (22) and memory interface (18), having a memory input, i.e., data (16) input to memory interface from input FIFO queue, and a memory output, i.e., output point from memory interface to multiplexor (20) as show in figure 1, the memory input is coupled to the tail output and the memory is operable to store the incoming data that is output from the tail output, and wherein the memory is operable to output the stored data at the memory output (figure 2, col. 2 lines 14-36 and lines 45-51), a multiplexer (20, figure 1) having first multiplexer input, i.e., input direct from input FIFO queue (14) as show in figure 1, and second multiplexer input, i.e., input from memory interface (18) as show in figure 1, the multiplexer having a control input, i.e., multiplexer control logic (24), to select one of the

multiplexer inputs to coupled to a multiplexer output (col. 2 lines 7-12, 14-36 and col. 3 lines 35-52), a heard FIFO memory, i.e., output FIFO queue (32, figure 1) having a head input coupled to the multiplexer output to receive the incoming data which either from input FIFO queue directly or from memory device as show in figure 1 and a head output to output the incoming data (col. 2 lines 7-12). Bass teaches the input FIFO queue is able to transfer incoming data to either output FIFO queue or memory device, wherein the determination is control by the controller, i.e., multiplexor control logic (24), write pointer, read pointer and comparator (col. 2 lines 21-29 and col. 3 line 53 through col. 4 line 6), in addition, Bass also teaches the memory interface (18) is able to store the contiguous addresses on the FIFO basis from the input FIFO queue (14) and (col. 2 lines 37-65), furthermore, Bass teaches inside the input FIFO including six different storage locations (40a-40f) wherein each storage location stores one data item and the data items are written at three data items from the input FIFO queue (14) to the DRAM (20) which under controlled by write pointer (44), read pointer (46) and comparator (48) and (col. 2 line 67 through col. 3 line 11) and Bass discloses the system further utilizes the head and tail pointers on contiguous addresses which further point out the edges the incoming data with selected size (col. 3 lines 23-33), thus, the controller coupled to the input FIFO and output FIFO, and the memory and operable to transfer one or more blocks of the income data having a selected block size from the input FIFO to the memory and from the memory to the output FIFO (col. 3 line 35 through col. 4 line 6 and col. 4 lines 29-43).

Regarding claim 2, Bass discloses the system wherein the head FIFO, i.e., output FIFO (32, figure 1) further comprises a head fill indicator coupled to the controller to indicate a fill characteristic of the head FIFO (col. 2 lines 21-32 and col. 3 line 65 through col. 4 line 3).

Regarding claim 3, Bass discloses the system wherein the controller transfers the one or more blocks of the incoming data having the selected block size from the input FIFO queue to the memory based on the output fill indicator (col. 2 lines 21-32, col. 3 line 65 through col. 4 line 3 and col. 4 lines 32-43).

Regarding claim 4, Bass discloses the system wherein the controller transfers the one or more blocks of the incoming data having the selected block size from the memory to the output FIFO queue based on the head fill indicator (col. 2 lines 29-36 and col. 3 lines 41-51).

Regarding claim 5, Bass discloses the system wherein the input FIFO queue further comprises a tail fill indicator, i.e., indicate the input FIFO queue is half full, empty, or complete full by writer pointer, read pointer and comparator (col. 2 line 66 through col. 3 line 12 and col. 3 line 53 through col. 4 line 3), coupled to the controller to indicate a fill characteristic of the input FIFO queue (col. 2 lines 24-36 and col. 3 lines 36-51).

Regarding claim 6, Bass discloses the system wherein the controller transfers the one or more blocks of the incoming data having the selected block size from the input FIFO queue to the memory based on the tail fill indicator, i.e., when the input FIFO indicates half full, (col. 24-36, col. 3 lines 41-51 and col. 4 lines 32-43).

Regarding claim 7, Bass discloses the data comprises data frames of varying length and where the one or more blocks are defined to include data from one or more of the data frames, and wherein a selected block may contain data from two or more data frames, i.e., the incoming data is fixed or selected size data, and the memory is able to reconstruct the oversize data when the amount of data being inputted exceeds the capacity or predetermined percentage of capacity of the input FIFO buffer and the output FIFO butter (col. 2 lines 32-65), in addition, Bass

discloses the system further utilizes the head and tail pointers on contiguous addresses which further point out the edges the incoming data with selected size (col. 3 lines 23-33), furthermore, Bass discloses the incoming data width will be variable which based on the particular application (col. 4 line 18-27).

Regarding claim 8, Bass discloses the system wherein the controller includes a control output coupled to the control input of the multiplexer (figure 2), wherein the controller is operable to control which of the multiplexer inputs is coupled to the multiplexer output (col. 2 lines 7-12, lines 14-32 and col. 3 lines 35-51).

Regarding claim 9, Bass discloses the system wherein a data path to the memory is wider than a width characteristic of the input FIFO queue, i.e., the bus between input FIFO queue and output FIFO queue having the same width, and the data from input FIFO queue to the output FIFO is one data at a time, and the data from input FIFO queue to the memory (20) is three data items at a time (col. 2 line 67 through col. 3 line 11 and col. 4 lines 7-27).

Regarding claim 10, Bass discloses a method for implementing a caching system, i.e., a bandwidth conserving queue manager (10, figure 1), the method comprising steps of receiving data at a tail FIFO memory, i.e., input FIFO queue (14, figure 1), (col. 1 line 66 through col. 2 line 3), selecting an efficiency level for operating a memory interface (col. 3 lines 23-33 and lines 53-64), determining a selected block size to support the efficiency level (col. 2 lines 32-36, col. 2 line 67 through col. 3 line 11 and col. 3 lines 23-33), transferring one or more blocks of the data having the selected block size from the input FIFO queue to the output FIFO queue when the output FIFO is within a first fill level, i.e., less than predetermine level, (col. 3 lines 36-41 and col. 4 lines 29-32), the output FIFO queue includes an output to output the data, i.e., output

data 34, (figure 1 and col. 2 lines 10-12), transferring the one or more blocks of the data having the selected block size, from the input FIFO queue to a memory (22, figure 1) via the memory interface (18, figure 1), when the output FIFO queue is within a second fill level, i.e., above predetermine level or full indication, (col. 2 lines 21-36, col. 3 lines 41-52 and col. 4 lines 32-43), transfer the one or more blocks of data from the memory to the output FIFO queue when the output FIFO queue is within a third fill level (col. 2 lines 29-51).

Regarding claim 11, Bass discloses the data comprises data frames of varying length, and the method further comprises a step of defining the one ore more blocks of data having the selected block size to include data from one or more of the data frames, and wherein a selected block of data may include data from two or more data frames, i.e., the incoming data is fixed or selected size data, and the memory is able to reconstruct the oversize data when the amount of data being inputted exceeds the capacity or predetermined percentage of capacity of the input FIFO buffer and the output FIFO butter (col. 2 lines 32-65), in addition, Bass discloses the system further utilizes the head and tail pointers on contiguous addresses which further point out the edges the incoming data with selected size (col. 3 lines 23-33), furthermore, Bass discloses the incoming data width will be variable which based on the particular application (col. 4 line 18-27).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pannell (US PAT. 6,510, 138) discloses network switch with head of line input buffer queue clearing (abstract).

Goodwin et al. (US PAT. 5,659,713) discloses memory stream buffer with variable-size pre-fetch depending on memory interleaving configuration (abstract).

Akada (4,958,299) discloses a control device for use with a drawing output unit, which selects from a plurality of image data stored in an image memory which corresponding to a set of drawings of various sizes (col. 2 lines 20-64).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tue-Fri 9:00 a.m. to 6:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Zhuo H. Li

September 5, 2003

MATTHEW KIM
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